

9/30/13

INFORMATION DISCLOSURE CITATION FORM FOR PATENT APPLICATION (FORM PTO-1449) (Substitute)			Docket No.: YOR920030139US1 Applicant(s): Chirag S. PATEL Filing Date: _____		Serial No.: 10/674, 331 Group: _____	
U.S. PATENTS						
Initials	Patent Number	Issue Date	Name	Class	Sub-class	Filing date
<div style="position: relative; width: 100%; height: 100%;"> </div>						
FOREIGN PATENT DOCUMENTS						
Initials	Document Number	Date	Country	Name	Translation? Yes/No/n/a	
<div style="position: relative; width: 100%; height: 100%;"> </div>						
OTHER DOCUMENTS (Title, Author, Date, Pages, Etc., if known)						
C.C.	S. Kiyono et al, Consideration of Chip Circuit Damages on DCS-FBGA Packages					
C.C.	Wu, L., Wang, Y. P., Hsiao C. S., "Innovative Stack-Die Package – S2BGA					
C.C.	M. Sunohara et al., Development of Wafer Thinning and Double-Sided Bumping					
C.C.	Technologies for the Three-dimensional Stacked LSI, all three presented at					
	52nd Electronic Components and Technology Conference, May 2002, San Diego, CA					
C.C.	Intel Stacked Chip Scale Packaging Products, available at					
	http://www.intel.com/design/flcomp/prodbref/298051.htm					
Examiner's Signature: <i>Chirag Patel</i>				Date Considered: 11/18/05		
Initial if reference was considered, whether or not citation is in conformance with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).						